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What is Claimed:

- 1 1. An semiconductor device, comprising:
2 a substrate having a source, a drain and a channel between said source and
3 said drain; and
4 a gate structure disposed over said channel, said gate structure having a
5 length of $1.25\text{ }\mu\text{m}$ or less and wherein the device does not include a lightly doped drain
6 region.
- 1 2. A semiconductor device as recited in claim 1, wherein said length is in
2 the range of approximately $0.25\text{ }\mu\text{m}$ to approximately $0.05\text{ }\mu\text{m}$.
- 1 3. A semiconductor device as recited in claim 1, wherein said gate
2 structure includes an oxide layer and said oxide layer has a thickness in the range of
3 approximately 1.5 nm to approximately 20.0 nm .
- 1 4. A semiconductor device as recited in claim 1, wherein a series
2 source/drain resistance exists in the device, and said series source/drain resistance per μm
3 of gate width is in the range of approximately $20\text{ }\Omega$ to approximately $100\text{ }\Omega$.
- 1 5. A semiconductor device as recited in claim 1, wherein the device is an
2 NMOSFET.
- 1 6. A semiconductor device are recited in claim 5, wherein said source and
2 said drain are doped n+ and said substrate is p-type.
- 1 7. A semiconductor device as recited in claim 1, wherein said source and
2 drain have a doping concentration in the range of approximately $1 \times 10^{20}\text{ atoms/cm}^3$ to
3 approximately $5 \times 10^{20}\text{ atoms/cm}^3$.
- 1 8. A semiconductor device as recited in claim 1, wherein the device is
2 PMOSFET.

1 9. A semiconductor device as recited in claim 8, wherein said source and
2 said drain are doped p+ and said substrate is n-type.

1 10. A semiconductor device as recited in claim 2, wherein said oxide layer
2 and said substrate form an interface and said interface is substantially planar and stress-
3 free.

1 11. A semiconductor device as recited in claim 1, wherein said channel
2 has a doping concentration of approximately $1 \times 10^{16}/\text{cm}^3$ to approximately $1 \times 10^{19}/\text{cm}^3$.

1 12. A field effect transistor, comprising:

2 a substrate having a source, a drain and a channel between said source and
3 said drain;

4 a gate structure including an oxide, which forms an interface with said
5 substrate, wherein said gate structure has a length in the range of approximately $0.05 \mu\text{m}$
6 to approximately $0.25 \mu\text{m}$ and the transistor does not include a lightly doped drain region.

1 13. A transistor as recited in claim 12, wherein said channel has a length
2 in the range of approximately $0.05 \mu\text{m}$ to approximately $0.25 \mu\text{m}$.

1 14. A transistor as recited in claim 12, wherein said oxide layer has a
2 thickness in the range of approximately 1.5 nm to approximately 20.0 nm .

1 15. A transistor as recited in claim 12, wherein a series source/drain
2 resistance exists in the transistor, and said series source/drain resistance is in the range of
3 approximately 20Ω to approximately 100Ω per μm of gate width.

1 16. A semiconductor device as recited in claim 12, wherein the device is
2 an NMOSFET.

1 17. A semiconductor device as recited in claim 16, wherein said source
2 and said drain are doped n+ and said substrate is p-type.

1 18. A semiconductor device as recited in claim 12, wherein said source
2 and drain have a doping concentration in the range of approximately 1×10^{20} atoms/cm³ to
3 approximately 5×10^{20} atoms/cm³.

1 19. A semiconductor device as recited in claim 12, wherein the device is
2 PMOSFET.

1 20. A semiconductor device as recited in claim 19, wherein said source
2 and said drain are doped p+ and said substrate is n-type.

1 21. A transistor as recited in claim 12, wherein said interface is
2 substantially planar and stress-free.

1 22. A semiconductor device as recited in claim 12, wherein said channel
2 has a doping concentration of approximately 1×10^{16} /cm³ to approximately 1×10^{19} /cm³.

1 23. A process for fabricating an integrated circuit, comprising:

2 forming a gate structure over a substrate, said gate structure having a
3 length of approximately 1.25 μ m or less; and

4 forming a source and a drain, said source and said drain not having lightly
5 doped regions.

1 24. A process for fabricating an integrated circuit as recited in claim 23,
2 wherein said process further comprises forming a channel before forming said source and
3 said drain.

1 25. A process as recited in claim 23, wherein said forming said gate
2 structure further comprises:

3 forming an oxide layer over said substrate; and

4 forming a conductive layer over said oxide layer.

1 26. A process as recited in claim 24, wherein said channel is doped by a
2 halo implantation.

1 27. A process as recited in claim 23, wherein said length is in the range of
2 approximately 0.25 μm to approximately 0.05 μm .

1 28. A process as recited in claim 25, wherein said oxide layer has a first
2 oxide portion and a second oxide portion.

1 29. A process as recited in claim 23, wherein a spacer is not formed
2 adjacent said gate structure.

1 30. A process as recited in claim 25, wherein said oxide layer has a
2 thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

1 31. A process as recited in claim 23, wherein said source and said drain
2 having doping levels in the range of approximately $1 \times 10^{20}/\text{cm}^3$ to $5 \times 10^{20}/\text{cm}^3$.

1 32. A process as recited in claim 24, wherein said channel has a doping
2 level in the range of approximately $1 \times 10^{16}/\text{cm}^3$ to approximately $1 \times 10^{19}/\text{cm}^3$.

1 33. A process for fabricating an integrated circuit, comprising:

2 forming an oxide layer over a substrate;

3 forming a conductive layer over said oxide layer, said oxide layer and said
4 conductive layer forming a gate having a length of 1.25 μm or less;

5 forming a channel in said substrate; and

6 forming a source and a drain, said source and said drain not having lightly
7 doped regions.

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1 34. A process as recited in claim 33, wherein said channel is doped by a
2 halo implantation.

1 35. A process as recited in claim 33, wherein said length is in the range of
2 approximately 0.25 μm to approximately 0.05 μm .

1 36. A process as recited in claim 33, wherein said oxide layer has a first
2 oxide portion and a second oxide portion.

1 37. A process as recited in claim 33, wherein a spacer is not formed
2 adjacent said gate structure.

1 38. A process as recited in claim 33, wherein said oxide layer has a
2 thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

1 39. A process as recited in claim 33, wherein said source and said drain
2 having doping levels in the range of approximately $1 \times 10^{20}/\text{cm}^3$ to approximately
3 $5 \times 10^{20}/\text{cm}^3$.

1 40. A process as recited in claim 33, wherein said channel has a doping
2 level in the range of approximately $1 \times 10^{16}/\text{cm}^3$ to approximately $1 \times 10^{19}/\text{cm}^3$.